attempts to reduce interference to CPU cycles during secondary bus transactions. The computer system includes a CPU and memory device coupled through a north bridge logic device. The computer also includes a south bridge logic device coupled to the north bridge by a primary bus. The south bridge waits as long as possible before asserting a flush request control signal to the north bridge. The south bridge asserts the flush request signal to the north bridge after a peripheral device coupled to the south bridge requests access to the primary bus to run a cycle. In an alternative embodiment, the invention includes a pair of south bridges where one south bridge is in a laptop computer and another south bridge is in an expansion base to which the laptop computer mates. The Wandler reference makes passing reference in column 6, lines 5-7 that the bridge logic 50 may be integrated into the CPU 25 but does not appear to say any more than this. In any vent, the office action alleges that the Wandler reference teaches all the claims elements of claims 1 and 28 but fails to disclose that memory access requests are processed by the north bridge at a rate of memory. Sakugawa has allegedly been cited for this proposition.

However, the Sakugawa reference does not teach what the Wandler reference is lacking. For example, the Sakugawa reference does not appear to be directed to a CPU and north bridge operation as required by the missing element and for this reason alone, the claims are in condition for allowance. Moreover, the office action cites to the CPU memory controller but the Sakugawa reference teaches slowing down access to the memory, which is contrary to Applicants' claimed invention. The system of Sakugawa utilizes a memory controller that performs access control to a built in memory in response to a request from a CPU. A wait count register stores a waiting period relating to the memory access. The memory controller then waits and then performs the memory access to the memory on behalf of the CPU. As such, memory access is actually slowed down in the Sakugawa reference as the CPU in the Sakugawa reference

does not access the memory at the rate of memory. For example, the claim requires processing, by the north bridge, the memory access request at a rate of memory. This limitation is not taught in Sakugawa since the cited portion refers to the CPU. In any event, the cited portion actually teaches an opposite approach from that claimed in that Applicants' claim processing, by the north bridge, memory requests at a rate of memory. The cited portions actually state that a waiting period is required and used from the time a memory access request is made to the time it is carried out which slows down memory access to and from the memory. As such, it appears that Sakugawa actually teaches lowering memory request rates to memory. Accordingly, the claims are believed to be in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

For example, claim 2 requires, among other things, it is alleged that the Wandler reference teaches integrating the south bridge on the substrate with a CPU and a north bridge. However, this cited section, namely column 6, lines 5-7, refers specifically only to the north bridge and it does not appear that Wandler contemplates integrating both a north bridge and a south bridge on the same chip, or substrate. In fact, Wandler teaches using a pair of south bridges that are actually in different products. Accordingly, this claim is also believed to be in condition for allowance. Claim 4 and others also add additional novel and non-obvious subject matter and Applicants respectfully reassert the relevant remarks made in previous responses.

Claims 5, 6, 32 and 33 stand rejected under 35 U.S.C. §103 as being unpatentable over Wandler in view of Sakugawa as applied to claims 1 and 28 and further in view of Onishi et al. Applicants respectfully reassert the relevant remarks made above and as such these claims are also believed to be in condition for allowance. Applicants also respectfully submit that the Onishi reference, namely column 10, lines 4-13 do not appear to describe translating, by the

north bridge, the address for virtual memory space to an address in physical memory space since the north bridge does not appear to be discussed in the cited section. As such, the claims are also believed to be in condition for allowance for this reason also.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance, and that a Notice of Allowance be issued in this application. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 2-3-05

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, IL 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005